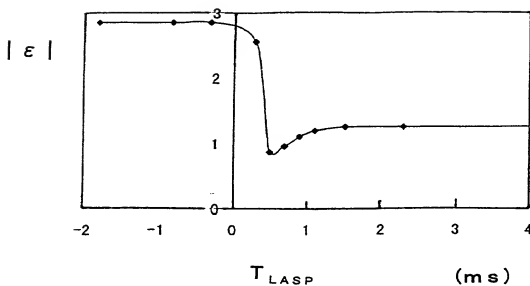


Fig. 1



\* "0 ms" : At Power Off State

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**F i g . 2**

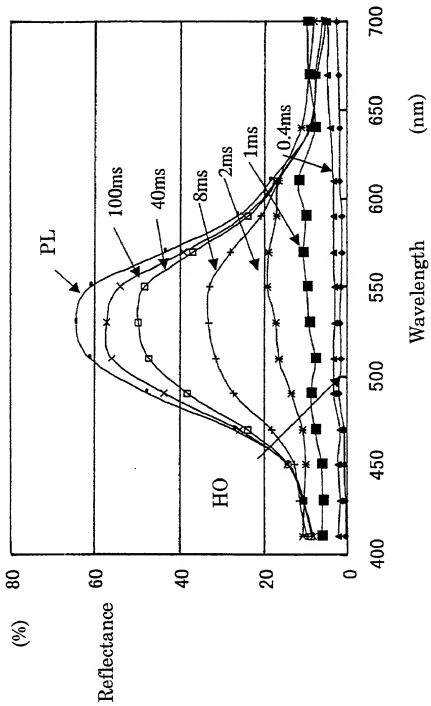


Fig. 3

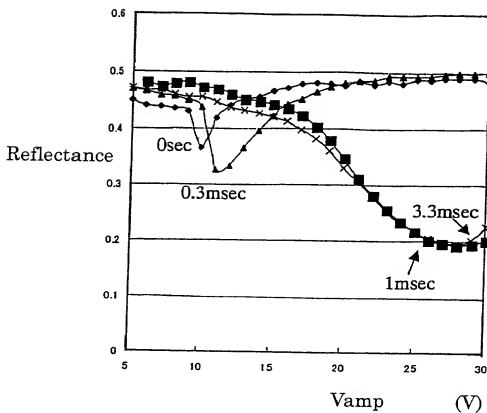


Fig. 4

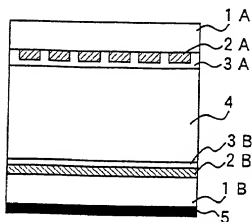


Fig. 5

T-pulse=13.2 ms

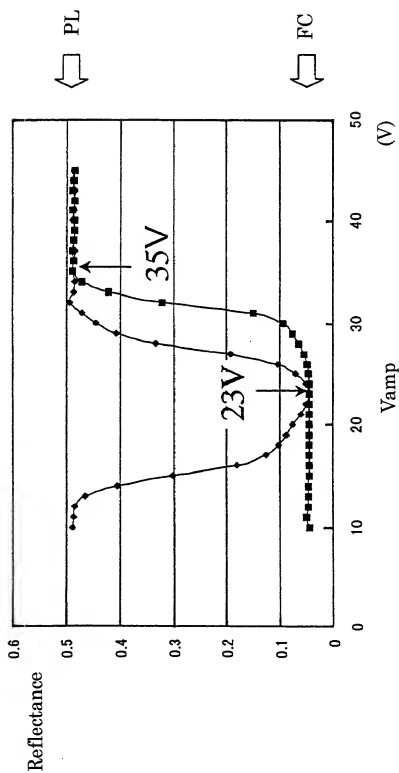


Fig. 6

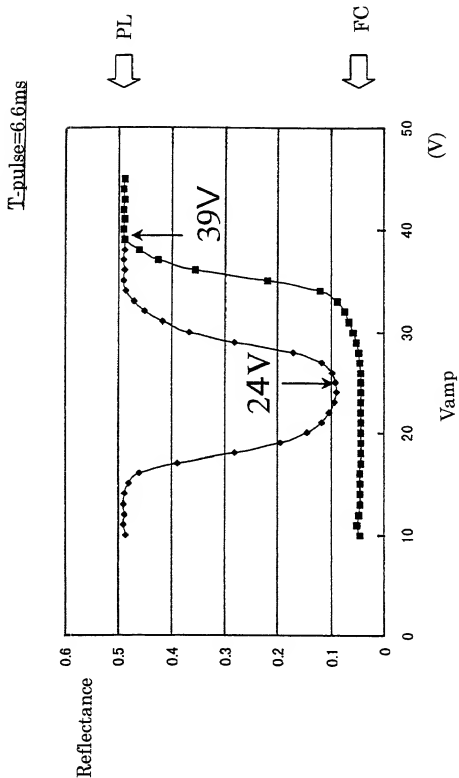


Fig. 7

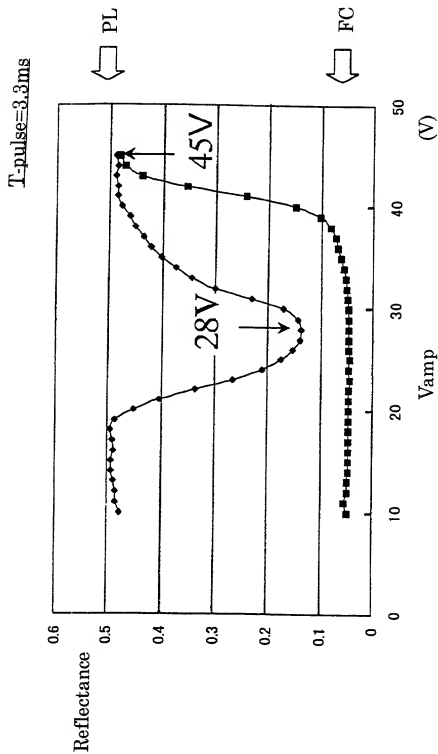


Fig. 8

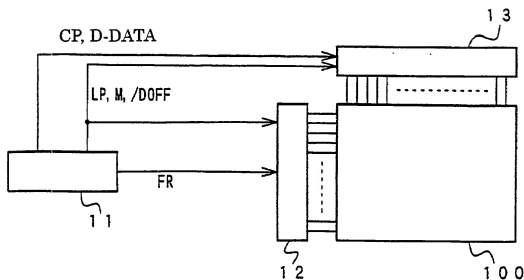


Fig. 9

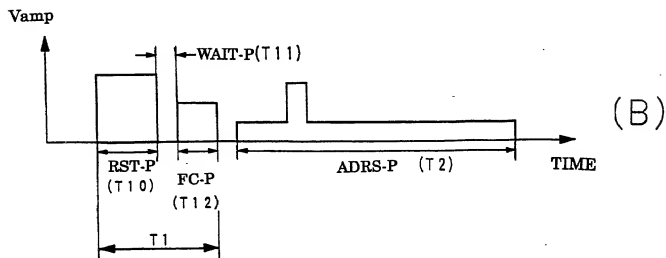
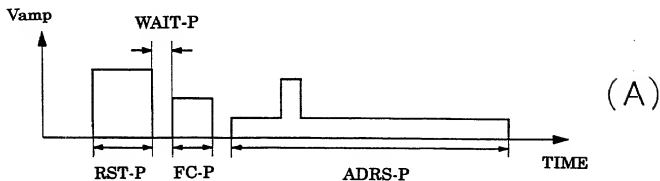


Fig. 10

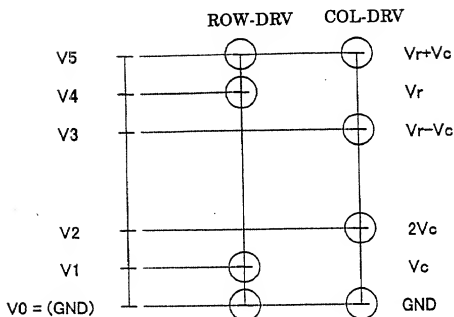


Fig. 11

ROW-DRV

/DOFF	M	SEL/NON-SEL	V-OUT
H	L	SEL	V5
H	H	SEL	V0
H	L	NON-SEL	V1
H	H	NON-SEL	V4
L	X	X	V0

COL-DRV

/DOFF	M	DATA	V-OUT
H	L	H	V0
H	H	H	V5
H	L	L	V2
H	H	L	V3
L	X	X	V0

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Fig. 12

FIG. 12

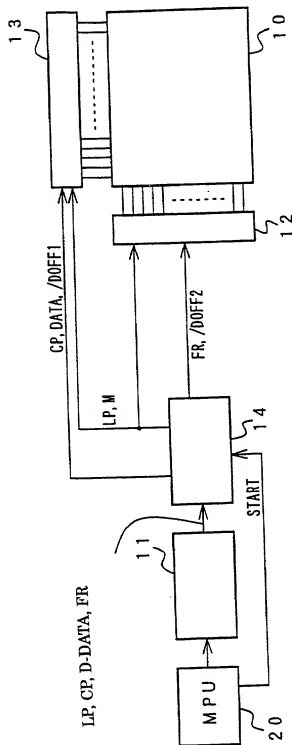


Fig. 13

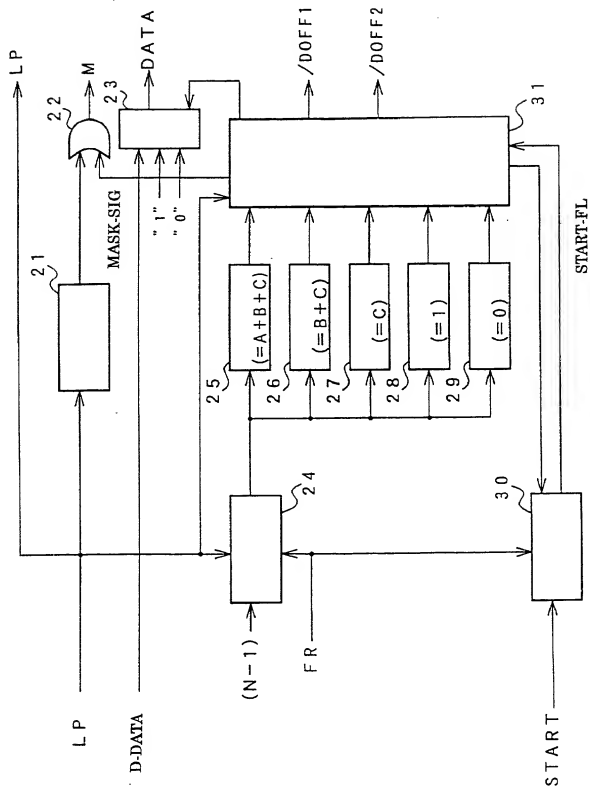


Fig. 14

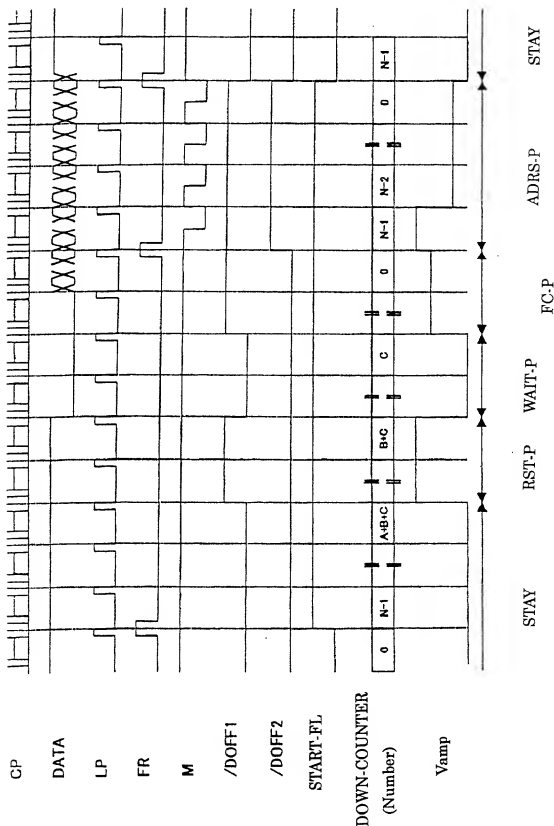


Fig. 15

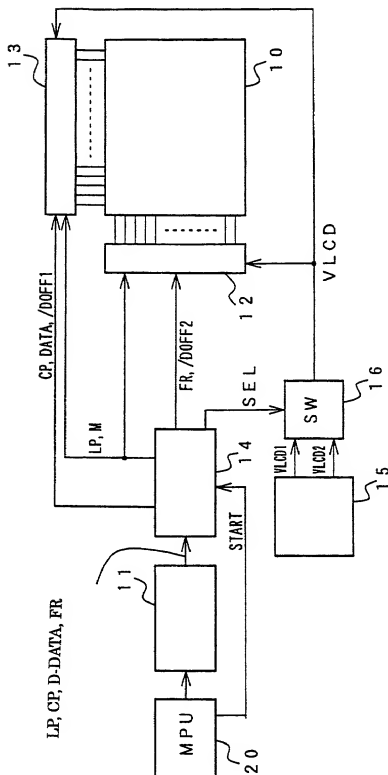


Fig. 16

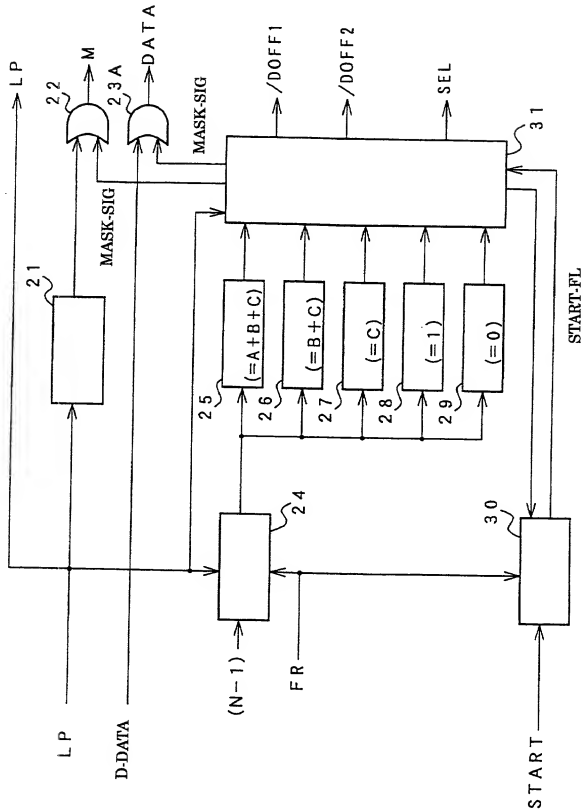
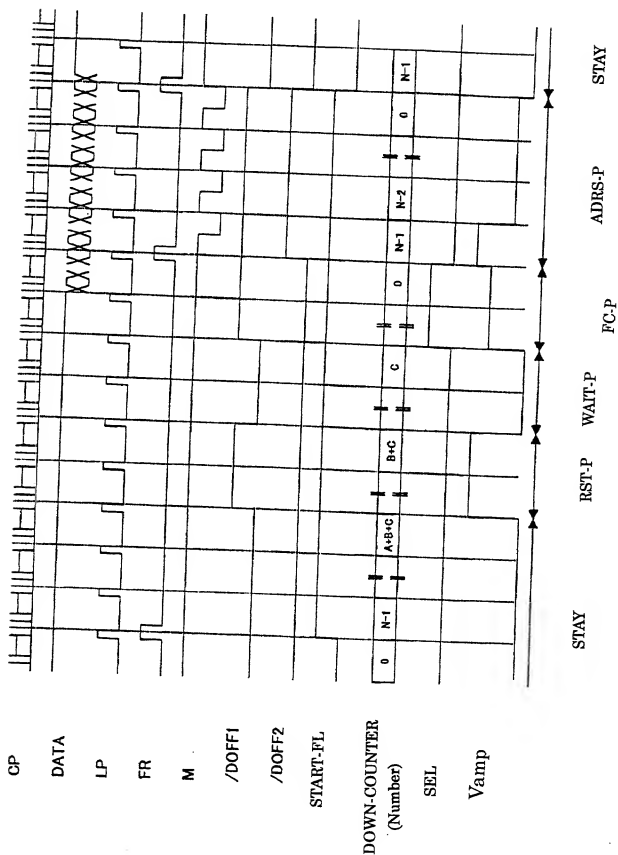


Fig. 17



F i g. 18

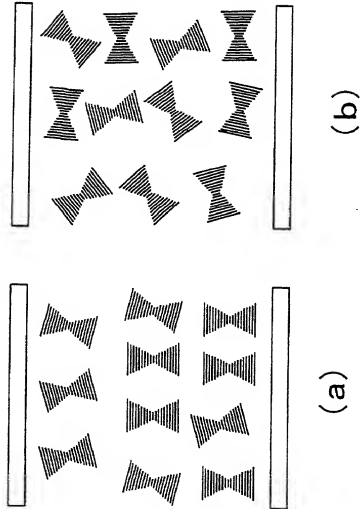


Fig. 19

Pulse width and times for establishing a FC state

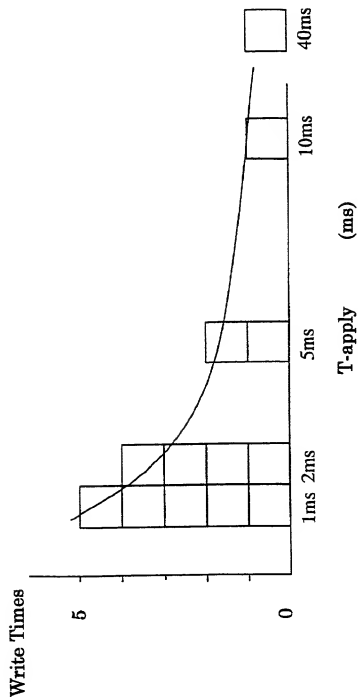




Fig. 20

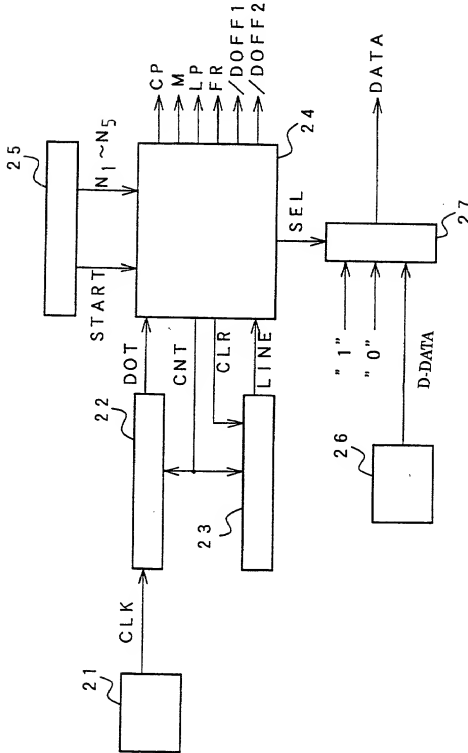


Fig. 21

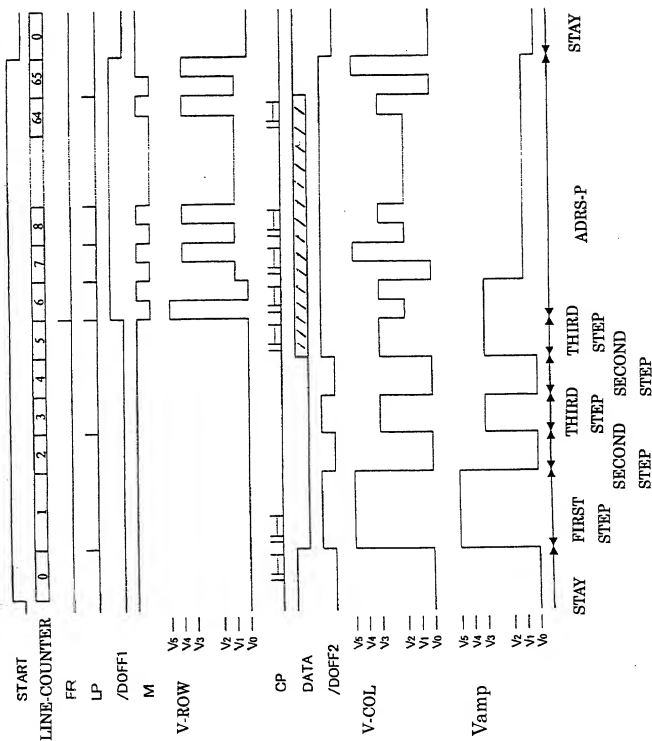


Fig. 22

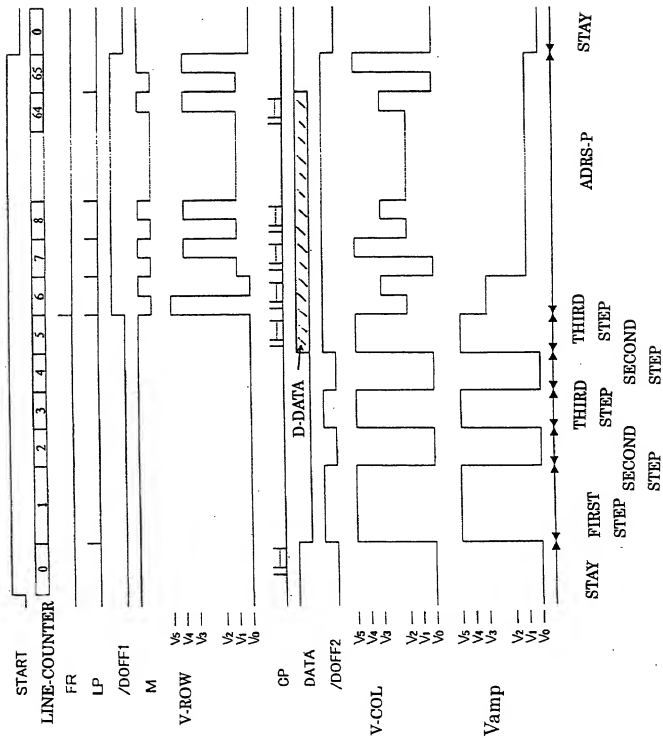


Fig. 23

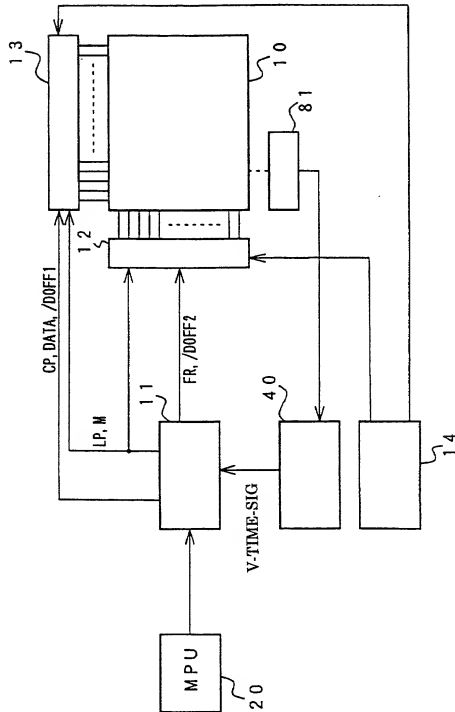


Fig. 24

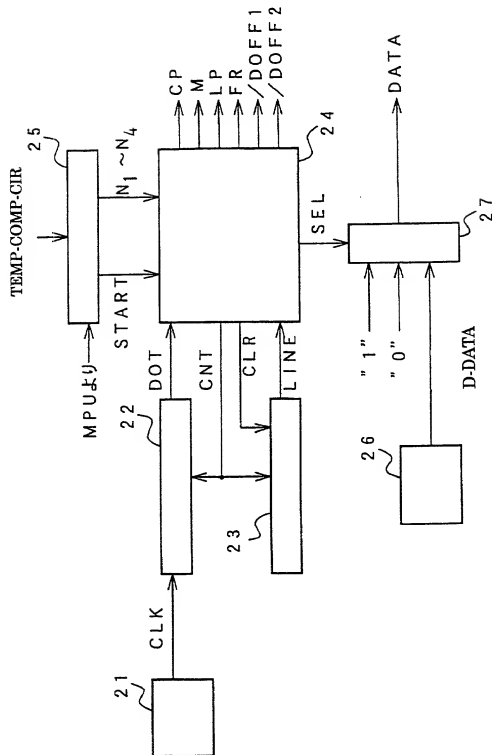


Fig. 25

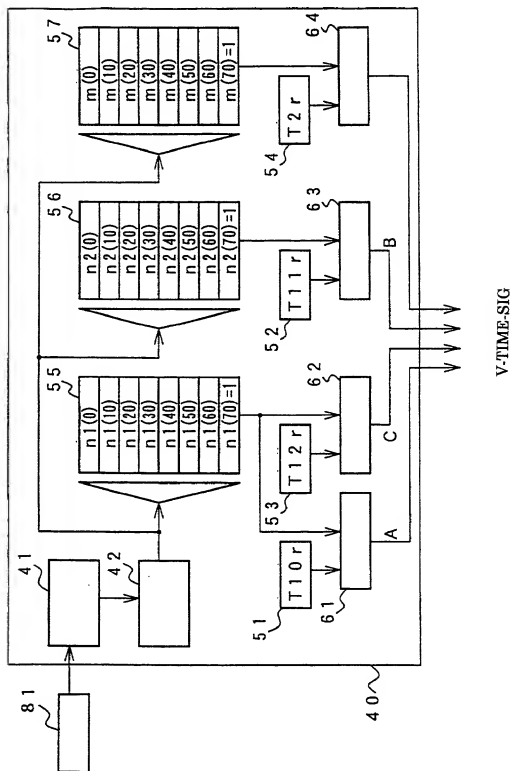
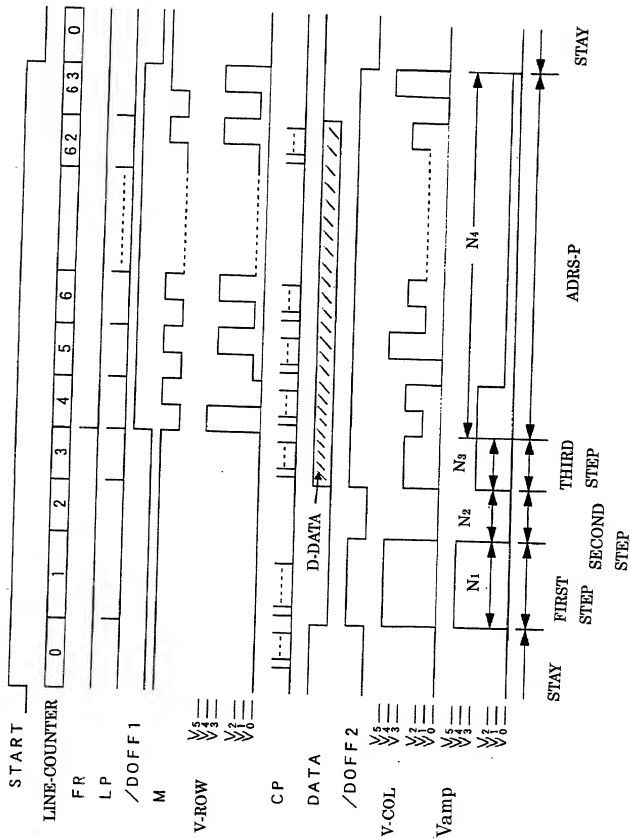
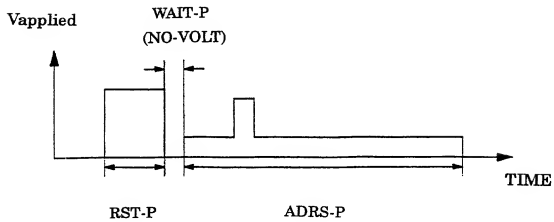


Fig. 26



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Fig. 28

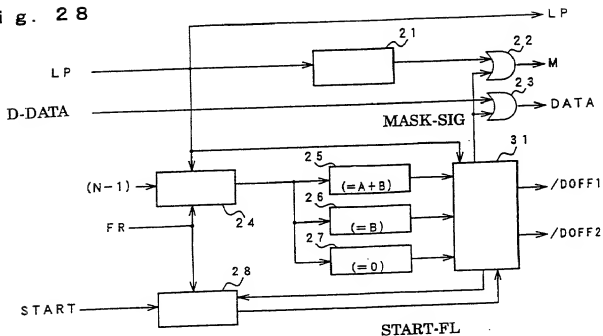
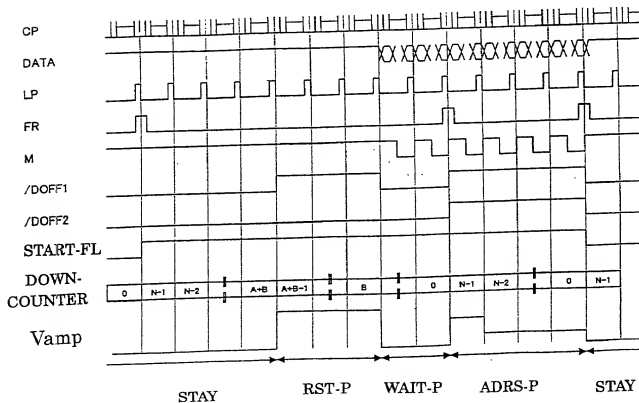
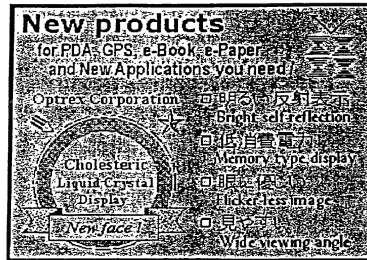


Fig. 29

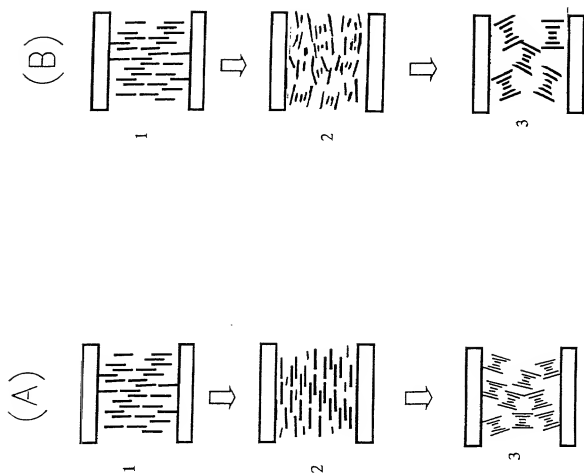


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F i g . 3 1



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